REMARKS

This Amendment is responsive to the Office Action dated July 8, 2005. All rejections and objections of the Examiner are respectfully traversed. Reconsideration and further examination are respectfully requested.

At paragraph 2 of the Office Action, the Examiner requested a concise explanation of the relevance of foreign reference DE3111991A1. The requested explanation will be provided in due course.

At paragraphs 4 through 16 the Examiner rejected claims 1 through 8 and 10 as being obvious under 35 U.S.C. 103, citing United States patent number 6,625,654 of Wolrich et al. ("Wolrich et al."), in combination with United States patent number 6,606,704 of Adiletta et al. ("Adiletta et al."). Applicants respectfully traverse this rejection.

As noted in the previous response, Wolrich et al. discloses a parallel, hardware-based multithreaded processor, including a general purpose processor that coordinates system functions, and a plurality of microengines that support multiple program threads. The Wolrich et al. processor also includes a memory control system that has a first memory controller that sorts memory references based on whether the memory references are directed to an even bank or an odd bank of memory, and a second memory controller that optimizes memory references based upon whether the memory references are read references or write references. A program thread communication scheme for packet processing is also described in Wolrich et al.

Adiletta et al. disclose a communication system including a parallel, hardware-based multithreaded processor coupled to a pair of busses and a memory system. The hardware-based multithreaded processor of Adiletta et al. includes multiple microengines 22 each with multiple

hardware controlled threads that can be simultaneously active and independently work on a task. See column 2, lines 56-67. As specifically described in Adiletta et al., the microengines operate with shared resources including the memory system and bus interfaces. See column 3, lines 28-42. As disclosed in column 8, lines 28-37, and illustrated in Fig. 3A of Adiletta et al., a microengine datapath in the Adiletta et al. system maintains a 5-stage micro-pipeline, which includes lookup of microinstruction words, formation of register file addresses, read of operands from register file, ALU, shift or compare operations, and write-back of results to registers. At column 18, lines 56-62, Adiletta et al. further disclose that an SRAM controller performs memory reference sorting to minimize delays (bubbles) in the pipeline from an SRAM interface to memory.

Nowhere in the combination of Wolrich et al. and Adiletta et al. is there disclosed or suggested any method or system for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process, including:

> providing a processor including a plurality of analysis machines and a plurality of computer resources, wherein each of said plurality of analysis machines includes an internal pipeline and is communicably coupled to a plurality of shared pipelines, ***wherein each said internal pipeline is an integer pipeline that starts the execution of every instruction that executes in said analysis machine in which it is included***;
>
> executing each instruction thread in one of the plurality of analysis machines; and
>
> sharing services of at least one of the plurality of computer resources between at least two of the plurality of analysis machines during the execution of each instruction thread. (emphasis added)

as in the present independent claim 1. . Analogous features are also present in the present independent claim 5. In contrast, the micro-pipeline cited by the Examiner in the microengines of Adiletta et al. is a datapath pipeline. Adiletta et al. specifically describe the micro-pipeline as follows beginning at line 28 of column 8:

> As shown in FIG. 3A, the microengine ***datapath*** maintains a 5-stage micro-pipeline 82. This pipeline includes ***lookup of microinstruction words*** 82a, ***formation of the register file addresses*** 82b, ***read of operands from register file*** 82c, ***ALU, shift or compare operations*** 82d, and ***write-back of results to registers*** 82e. (emphasis added)

The above description provides no hint or suggestion of even the desirability of having an integer pipeline that starts the execution of every instruction that executes in the analysis machine in which it is included, as in the present independent claims 1 and 5.

For the above reasons, Applicants respectfully urge that the combination of Wolrich et al. and Adiletta et al. does not disclose or suggest all the features of the present invention as set forth in independent claims 1 and 5. Accordingly, the combination of Wolrich et al. and Adiletta et al. does not render the present independent claims 1 and 5 obvious under 35 U.S.C. 103. As to dependent claims 2-4, 6-8, and 10, they each depend from independent claims 1 and 5, and are respectfully believed to be patentable over the combination of Wolrich et al. and Adiletta et al. for at least the same reasons.

At paragraphs 17-26 of the Office Action, the Examiner rejected claims 9 and 11-18 for obviousness under 35 U.S.C. 103, again citing Wolrich et al. and Adiletta et al., and additionally citing United States patent number 6,081,860 of Bridges et al. ("Bridges et al."). Applicants respectfully traverse this rejection.

As noted in the previous response, Bridges et al. disclose a process and system in which master and slave devices are connected by a single address bus, a write data bus and a read data bus. The arbiter device of Bridges et al. receives requests for data transfers from the master devices and selectively transmits the requests to the slave devices. The design of the Bridges et al. system is configured to advantageously function in mixed systems which may include

address-pipelining and non-address-pipelining slave devices. The relevant teachings of Wolrich et al. and Adiletta et al. are discussed above with regard to the rejections in paragraphs 4-16 of the Office Action.

Nowhere in the combination of Wolrich et al., Adiletta et al. and Bridges et al. is there disclosed or suggested any system for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process, including:

> providing a processor including a plurality of analysis machines and a plurality of computer resources, wherein each of said plurality of analysis machines includes an internal pipeline and is communicably coupled to a plurality of shared pipelines, ***wherein each said internal pipeline is an integer pipeline that starts the execution of every instruction that executes in said analysis machine in which it is included;***
>
> executing each instruction thread in one of the plurality of analysis machines; and
>
> sharing services of at least one of the plurality of computer resources between at least two of the plurality of analysis machines during the execution of each instruction thread. (emphasis added)

as in the present independent claim 5, from which dependent claims 9 and 11-18 depend. As noted above, Wolrich et al. teaches a system for parallel processing that is an alternative to a pipelined machine, and Adiletta et al. describe a specific type of datapath micro-pipeline. Bridges et al. describe a technique for enhancing a processor local bus to allow for address pipelining, but also provide no hint or suggestion of any method or system for providing analysis machines each including an internal pipeline ***wherein each internal pipeline is an integer pipeline that starts the execution of every instruction that executes in the analysis machine in which it is included,*** as in the present independent claim 5. Thus the combination of Wolrich et al., Adiletta et al. and Bridges et al. provides no teaching of significant features of the present independent claim 5.

For the above reasons, Applicants respectfully urge that the combination of Wolrich et al., Adiletta et al. and Bridges et al. fails to disclose or suggest all the features of the present independent claim 5, from which claims 9 and 11-18 depend. Accordingly, the combination of Wolrich et al., Adiletta et al. and Bridges et al. does not support a *prima facie* case of obviousness under 35 U.S.C. 103 with regard to the present independent claim 5, and/or dependent claims 9 and 11-18. Dependent claims 9 and 11-18 would therefore not be obvious to one skilled in the art. Reconsideration of all pending claims is respectfully requested.

For these reasons, and in view of the above amendments, Applicants respectfully request that all rejections and objections of the Examiner be withdrawn. The application is now considered to be in condition for allowance, and such action is earnestly solicited.

Applicants have made a diligent effort to place the application in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone David A. Dagg, Applicants' Attorney at 978-264-6664 so that such issues may be resolved as expeditiously as possible.

Respectfully Submitted,

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Date

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